WHAT IS CLAIMED IS

1. An operation method for non-volatile memory, comprising the steps of:

providing a non-volatile memory cell capable of storing at least a first bit and a second bit and having a first region and a second region with a channel therebetween and a gate above the channel but separated therefrom by a charge trapping layer sandwiched between a first dielectric layer and a second dielectric layer, wherein the first bit and the second bit are positioned close to the first and second regions respectively;

determining a first programmed voltage for the first bit, a second programmed voltage for the second bit and an erased voltage for the first and second bits, wherein the first programmed voltage is smaller than the second programmed voltage;

reading the first bit by applying a voltage to the second region; and

reading the second bit by applying a voltage to the second region, wherein the voltage applied to the second region for reading the second bit is smaller than that for reading the first bit.

2. The operation method for non-volatile memory in accordance with Claim 1, wherein the voltage applied to the second region for reading the first bit is so large that a depletion region around the second region is induced and whether the second bit is programmed or not is ignored.

3. The operation method for non-volatile memory in accordance with Claim 1, wherein a voltage is further applied to the gate for reading the first bit, and the voltage applied to the gate for reading the first bit is between the erased voltage and the first programmed voltage.

4. The operation method for non-volatile memory in accordance with Claim 1, wherein a voltage is further applied to the gate for reading the second bit, and the voltage applied to the gate for reading the second bit

is between the first programmed voltage and the second programmed voltage.

5. The operation method for non-volatile memory in accordance with Claim 1, wherein the voltage applied to the second region for reading the second bit is between 0.1 and 0.5 volts.

6. The operation method for non-volatile memory in accordance with Claim 1, wherein the voltage applied to the second region for reading the first bit is between 0.6 and 2 volts.

7. The operation method for non-volatile memory in accordance with Claim 1, wherein the first programmed voltage is between 2 and 4 volts.

8. The operation method for non-volatile memory in accordance with Claim 1, wherein the second programmed voltage is between 4 and 6 volts.

9. The operation method for non-volatile memory in accordance with Claim 1, wherein the erased voltage is between 0.5 and 2 volts.

10. The operation method for non-volatile memory in accordance with Claim 1, wherein the charge trapping layer is composed of silicon nitride.

11. The operation method for non-volatile memory in accordance with Claim 1, wherein the non-volatile memory cell is of N-type.

12. The operation method for non-volatile memory in accordance with Claim 1, wherein the non-volatile memory cell is a vertical memory cell.